WE CLAIM:

1. A circuit comprising:

a plurality of mixed-signal outputs;

a first set of driving elements connected together in sequence each having a respective output connected to a respective one of the mixed-signal outputs, the first set of driving elements having a first driving element and having a last driving element;

a second set of driving elements connected together in sequence each having a respective output connected to a respective one of the mixed signal outputs in an order opposite to an order of connection of the first set of driving elements to the mixed signal outputs, the second set of driving elements having a first driving element and a last driving element;

wherein while in a first control state the first set of driving elements drives each of the mixed-signal outputs towards a respective off state sequentially in a direction from the first driving element of the first set towards the last driving element of the first set such that any mixed-signal output that is driven only partially towards its respective off state maintains an analog value; and

wherein while in a second control state the second set of driving elements drives each of the mixed-signal outputs towards a respective on state sequentially in a direction from the first driving element of the second set towards the last driving element of the second set such that any mixed-signal output that is driven only partially towards its respective on state maintains an analog value;

wherein while in a third control state each mixed-signal value maintains its respective value.

2. The circuit of claim 1 comprising two control inputs that define the first, second and third control states.

3. The circuit of claim 1 wherein each driving element is a tri-state buffer, and each of the on states are represented by a high voltage, and each of the off states are represented by a low voltage.

4. The circuit of claim 1 wherein each driving element is an inverter, and each of the on states alternate between being represented by a low voltage and a high voltage, and each of the off states alternate between being represented by a high voltage and a low voltage.

5. The circuit of claim 1 further comprising:

a logic on biasing circuit that biases an on voltage of any active high control input to an amount below logic high and/or biases any active low control input to an amount above logic low.

6. The circuit of claim 1 further comprising:

a logic off biasing circuit that biases an off voltage of any active high control input to an amount above logic low and/or biases any active low control input to an amount below logic high.

7. The circuit of claim 1 wherein:

each driving element is a single-transition driving element.

8. The circuit of claim 1 further comprising a tuneable filter connected between the control input(s)and the driving elements.

9. The circuit of claim 1 further comprising:

a respective additional filter connected to each of the mixed-signal outputs.

10. The circuit of claim 1 further comprising circuitry to dynamically determine a sub-set of the mixed-signal outputs that include at least those producing analog value outputs.

11. The circuit of claim 10 further comprising:

at least one additional filter;

circuitry that dynamically connects the at least one additional filter to mixed-signal outputs that are outputting analog values.

12. The circuit of claim 11, wherein the at least one filter has at least one dynamically adjustable filter characteristic.

13. The circuit of claim 1 further comprising:

circuitry for detecting when a particular mixed-signal output has reached a digital state, and for dynamically securing the particular mixed-signal output to an appropriate reference upon making such a detection.

14. The circuit of claim 1 further comprising:

circuitry for maintaining an approximate state of the mixed-signal outputs upon power down or idle modes of the circuit.

15. The circuit of claim 10 further comprising:

at least one state maintaining element for maintaining an approximate state of the mixed-signal outputs upon power down or idle modes of the circuit;

circuitry to dynamically connect the at least one state maintaining element to the mixed-signal outputs determined to be outputting analog values.

16. The circuit of claim 14 wherein the circuitry for maintaining the approximate state of the mixed signal-outputs which maintains a reduced number of states from which the entire approximate state can be deduced.

17. The circuit of claim 1 adapted to receive at least one control input, the circuit further comprising steering logic for directing signals received on the at least one control input to a subset of the circuit generating analog values.

18. The circuit of claim 1 further comprising a delay line comprising at least one delay element, wherein each mixed-signal output controls how much delay such elements introduce into the delay line.

19. The circuit of claim 1 further comprising an LC oscillator, wherein each mixed-signal output is used to tune capacitance of the LC oscillator.

20. A delay locked loop synchronization circuit comprising the circuit of claim 1.

21. A phase locked loop synchronization circuit comprising the circuit of claim 1.

22. A clock de-skew circuit comprising the circuit of claim 1.

23. A circuit implemented method comprising:

in a first control state, driving each of a set of mixed-signal outputs towards a respective off state sequentially from a first mixed signal output towards a last mixed-signal output such that any mixed-signal output that is driven only partially towards its respective off state maintains an analog value; and

in a second control state, driving the mixed-signal outputs towards a respective on state sequentially from the last mixed-signal output towards the first mixed-signal output such that any mixed-signal output that is driven only partially towards its respective on state maintains an analog value.

24. The circuit implemented method of claim 23 further comprising dynamically determining a subset of the set of mixed-signal outputs including at least those that are outputting an analog value.

25. The circuit implemented method of claim 24 wherein dynamically determining which of the set of mixed-signal outputs are outputting an analog value comprises:

for at least one mixed-signal output:

receiving at least one neighbouring mixed-signal outputs;

determining the mixed-signal output is analog if the neighbouring mixed-signal output(s) are consistent with the particular mixed-signal output being an analog value for a mixed-signal thermometer code.

26. The circuit implemented method of claim 25 further comprising:

dynamically connecting at least one additional filter to the mixed-signal outputs that are outputting analog values.

27. The circuit implemented method of claim 25 further comprising maintaining a respective state for each of the mixed-signal outputs that are outputting analog values.

28. The circuit implemented method of claim 23 further comprising:

detecting when a particular mixed-signal output has reached a digital state;

upon detecting that a particular mixed-signal output has reached a digital state, securing the particular mixed-signal output to an appropriate reference.

29. The circuit implemented method of claim 28 wherein detecting when a particular mixed-signal output has reached a digital state comprises:

receiving at least one neighbouring mixed-signal outputs; determining if the neighbouring mixed-signal outputs are consistent with the particular mixed-signal output being a digital state for a thermometer code.

30. The circuit implemented method of claim 23 further comprising:

receiving at least one control input;

producing at least one biased control input by biasing an on voltage of any active high control input to an amount below logic high and/or biasing any active low control input to an amount above logic; and

the control state being determined by the at least one biased control input.

31. The circuit implemented method of claim 23 further comprising:

receiving at least one control input;

producing at least one biased control input by biasing an off voltage of any active high control input to an amount above logic low and/or biasing any active low control input to an amount below logic high; and

the control state being determined by the at least one biased control input.

32. The circuit implemented method of claim 23 further comprising:

controlling an amount of delay introduced by a respective at least one delay element in a delay line with each of the mixed-signal outputs.

33. A circuit comprising:

at least one control input defining at least a first control state and a second control state;

a plurality of mixed-signal outputs each characterized by a respective on state, a respective off state, and a respective analog range;

a set of circuit elements connected to cause sequential transitions of any mixed-signal output that is in a respective off state or in the respective analog range towards a respective on state during a first control state, and to cause sequential transitions of any mixed-signal output that is in a respective on state or in the respective analog range towards a respective off state during a second control state.

34. The circuit of claim 33 wherein the on states are all logic high and the off states are all logic low.

35. The circuit of claim 33 wherein the on states alternate between being logic high and logic low, and the off states alternate between being logic low and logic high.

36. A method for dynamically determining if a particular output of a set of mixed-signal outputs representing a mixed signal code is outputting an analog value, the method comprising:

receiving at least one neighbouring mixed-signal outputs;

determining if the neighbouring mixed-signal outputs are consistent with the particular mixed-signal output being an analog value for the mixed-signal code.

37. The method of claim 36 wherein the mixed-signal code is a thermometer code.

38. The method of claim 36 further comprising:

dynamically connecting at least one additional capacitance or filter stage to the mixed-signal outputs that are outputting analog values.

39. The method of claim 36 further maintaining a respective state for each of the mixed-signal outputs that are outputting analog values.

40. A method for processing a set of mixed-signal outputs, the method comprising:

detecting when a particular mixed-signal output has reached a digital state;

upon detecting that a particular mixed-signal output has reached a digital state, securing the particular mixed-signal output to an appropriate reference.

41. The method of claim 40 wherein the set of mixed-signal outputs represent a mixed-signal code, and wherein detecting when a particular mixed-signal output has reached a digital state comprises:

receiving at least one neighbouring mixed-signal outputs;

determining if the neighbouring mixed-signal outputs are consistent with the particular mixed-signal output being a digital state for the mixed-signal code.

42. A delay lock loop circuit comprising:

a phase detector receiving a reference signal and a feedback signal and having an UP output signal and a DOWN output signal;

an asynchronous dual mixed signal shift register receiving said UP output signal and said DOWN output signal;

a delay line subcircuit having a plurality of delay elements and receiving said reference signal and outputs of said asynchronous dual mixed signal shift register, said delay line subcircuit producing said feedback signal;

wherein:

said mixed signal thermometer filter having a plurality of control nets, each control net producing one output of said asynchronous dual mixed signal shift register, each output of said asynchronous dual mixed signal shift register being coupled to one of said plurality of delay elements in said delay line subcircuit;

said UP output signal and said DOWN output signal affects said plurality of control nets to increase or decrease a delay in said delay line subcircuit;

each delay element has an associated capacitance which directly affects said delay through said delay line.

43. A circuit according to claim 41 wherein

said asynchronous dual mixed signal shift register comprises dual parallel lines of cascaded circuit elements, one of said dual parallel lines of cascaded circuit elements receiving said UP output signal and the other of said dual parallel lines of cascaded circuit elements receiving said DOWN output signal.

44. A circuit according to claim 43 wherein one line of said dual parallel lines is coupled to Vss and said other line is coupled to Vdd.

45. A circuit according to claim 43 wherein each one of said cascaded circuit elements produces an output of said shift register and is coupled to a specific one of said plurality of control nets.

46. A circuit according to claim 45 wherein each one of said cascaded circuit elements is a tri-state buffer.

47. A circuit according to claim 45 wherein each one of said cascaded circuit elements is an inverter.

48. A circuit according to claim 41 wherein each delay element contributes to a total delay through said delay line.

49. A circuit according to claim 48 wherein each delay element comprises at least one transistor.

50. A circuit according to claim 49 wherein each of said at least one transistor is a drain-connected transistor with a source lead which is physically unconnected.